UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,118	02/25/2004	Osamu Kimura	1075.1253	1980

21171 7590 12/11/2007
STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
WALTER, CRAIG E	

ART UNIT	PAPER NUMBER
2188	

MAIL DATE	DELIVERY MODE
12/11/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/785,118	Applicant(s) KIMURA ET AL.	
	Examiner Craig E. Walter	Art Unit 2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,9-13,15-18,23-27 and 29-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,9-13,15-18,23-27 and 29-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 31 October 2007 has been entered.

Status of Claims

2. Claims 1-4, 9-13, 15-18, 23-27 and 29-33 are pending in the Application.

Claims 1, 13, 15, 27 and 29-32 have been amended.

Claim 33 is new.

Claims 5-8, 14, 19-22 and 28 have been cancelled.

Claims 1-4, 9-13, 15-18, 23-27 and 29-33 are rejected.

Response to Amendment

3. Applicant's amendments and arguments filed on 31 October 2007 in response to the office action mailed on 31 July 2007 have been fully considered, but they are not persuasive. Therefore, the rejections made in the previous office action are maintained, and restated below, with changes as needed to address the amendments.

Claim Objections

4. Claim 31 is objected to because of the following informalities:

As for claim 31, the limitation "the first management module of controlling the master area of the first management module and the mirror area of the second management module" (lines 7-8) should be changed to "the first management module controls the master area of the first management module and the mirror area of the second management module" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 31 is rejected under 35 U.S.C. 102(b) as being anticipated by Sicola et al. (US Patent 6,279,078 B1), hereinafter Sicola.

As for claim 31, Sicola teaches an apparatus comprising:

a host interface module controlling an interface to an external device, the host interface module producing an address designation (Fig. 1, element 12 - the host interface is connected to the external host CPU to the controller which helps to determine where the data is to be written into the cache - col. 2, lines 52-61);

a plurality of management modules each having a cache memory (Fig. 2A, each controller has a respective cache, the “this controller” can write data into either its own cache, or the “other controller’s” cache), at least two of the plurality of management modules set in mirror relation to each other (col. 3, lines 18-41 – the caches are in mirror relations to each other), a data written to a master area of a first management module simultaneously written to a mirror area of a second management module, the first management module of controlling the master area of the first management module and the mirror area of the second management module (again referring to col. 3, lines 18-44, the data is written simultaneously into each of the cache memories via cache mirroring); and

a bridge module connecting the host interface module and the plurality of management modules, without connecting through any other bridge modules, the bridge module producing address information for two transferred-to addresses for the data written to the at least two management modules of the plurality of management modules (Fig. 1, element 28,– the bus exchanger is a "bridge module" which allows access to all remaining elements of the controller (including notably the host interface and the cache - col. 2, line 52 through col. 3, line 4. In order to access the cache memories, all information (data, control, addressing) must come from the bus exchanger).

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 32 and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Avraham et al. (US PG Publication 2004/0103238 A1), hereinafter Avraham.

As for claim 32, Avraham teaches a method of efficiently using a mirrored cache, the method comprising:

> determining whether a master area of a first memory module is insufficient for a data input request; and storing data initially directed to the master area, from said data input request, of a first memory module in a mirror area of a second memory module (paragraph 0054, all lines – Avraham teaches a second memory module as being written with all or part of a first memory module's data once it is determined that the first memory module is full - paragraph 0054, all lines). Simply stated, Avraham teaches a second memory module as being written with all of part of a first memory module's data once it is determined that the first memory module is full. Note, the data being transmitted from the first memory module to the second was "initially" directed to the master area (i.e. stored there prior to be sent to the second memory).

More specifically (referring again to paragraph 0054, all lines), the determining step is met once the system checks to see if the cache is full. That is, every time a new write request is received, the cache is checked to see if it is full (see Fig. 3). The storing step is met by Avraham's process step of transferring data from the volatile memory to

the nonvolatile memory. That is, data that is stored in the volatile memory was originally "from the data input request" for it to be stored in the volatile memory, therefore the data stored in the nonvolatile memory (after the transfer from volatile to nonvolatile memory is complete) comprises data once directed to the master area of the first memory, from the data input request from which a determination was made to see if the master area of the volatile memory was "sufficient".

As for claim 33, Avraham teaches a storage control method comprising:

transferring data to two cache modules using two transferred-to addresses (paragraph 0054, all lines – data is transferred to a volatile memory, and subsequently to a non-volatile memory. The system must inherently use addressing information in order to access the memory locations, hence Avraham's method includes "using two transferred-to addresses") and;

storing data, from a data input request in a mirror area of one cache module, when a master area of the other cache module is insufficient for the data input request (paragraph 0054, all lines – Avraham teaches a second memory module as being written with all or part of a first memory module's data once it is determined that the first memory module is full - paragraph 0054, all lines).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 13, 15, 27, 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Weber (US Patent 5,937,174) in view of Hauck et al. (US PG Publication 2003/0158999 A1), hereinafter Hauck, and in further view of Avraham (US PG Publication 2004/0103238 A1).

As for claims 13, 27, and 30, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, combination of elements 204 and 206);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface modules, without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module (Fig. 2, element 208 – the connections between the memory and the host are busses 252 and 250), the bridge module producing address information for two transferred-to addresses for the data written to the at least two second modules of the plurality of second modules – note data, commands and addressing information must be sent through the bus bridge

(208) to reach the disks. In other words, the addressing information is "produced" by the bus bridge before it reaches the memory).

said host interface module and said management modules for data transfer among said modules, said host interface module writing data to be written, which is received from said host, through said bridge module into cache memories of two of said plurality of management modules (referring again to Fig. 2, the host can communicate with the storage module (element 104, which contains multiple modules or drives) via the host interface, the bridge and the disk interfaces (combination of elements 204 and 206, 208 and 138.1 respectively)) - col. 7, line 47 through col. 8, lines 39. It is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as will be discussed *infra*.

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ... 118). Referring to Fig. 2, each control unit (i.e. controller) contains a Read Write Cache Area, and a Cache Copy Area – paragraph 0039, all lines. Since Hauck's controllers inherently controller access to the storage system, they assert at least some control over the control system.

Weber additionally fails to teach the management modules as containing cache with the ability to mirror data, however Hauck teaches each of said management modules including management means (each controller is used to manage read/write functions to the cache) for managing information on the management module which is in mirror relation to this management module (referring to Fig. 2, Host Write #1 data (230) is written to controller 2 (i.e. mirrored), and likewise Host Write #2 data (270) is mirrored to controller 1 – paragraph 0039-0040 all lines). Hauck additionally teaches managing the association between a master area address in said cache memory in this management module and a mirror area address in said cache memory of the management module being in the mirror relation to this management module (referring to Fig. 4, a master area for each cache is maintained (Read/Write/Copy Cache)). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers

to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Hauck additionally teaches in a case in which a capacity of a master area of said cache memory of the one second module is full when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory of the one second management module, the one second management module preserves the readout data in a mirror area of said cache memory of the other second management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

Lastly, neither Hauck nor Weber teach a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time a mirror area of said one second module are written.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

As for claims 1, 15, and 29, Weber teaches a storage control apparatus placed between a disk unit and a host for controlling access to said disk unit by said host, said storage control apparatus comprising:

a disk interface module for controlling an interface to said disk unit (Fig. 2, element 138.1);

a host interface module for controlling an interface to said host (Fig. 2, the combination of elements 204 and 206);

Weber further teaches:

a bridge module connected through an interface bus to said disk interface module without connecting through any other bridge modules, said host interface module and said management modules for making connections among said disk interface module, said host interface module and said management modules for data transfer among said modules (Fig. 2, element 208 – the connections between the memory and the host are busses 252 and 250),

said bridge module including:

address production means for analyzing said addressing information, which is received together with said data to be written from said host interface module, to produce two transferred-to addresses for designation of said two management modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories (col. 8, lines 20-39) – the bridge unit works in conjunction with the host interface and the memory controller. The bridge unit receives data and address from the host

interface and memory controller in order to communicate with (i.e. perform memory access functions on) the memory subsystem. The interface and memory controller help to permit the bridge to get the correct data to the correct locations on the disks within the subsystem. Note data, commands and addressing information must be sent through the bus bridge (208) to reach the disks. In other words, the addressing information is "produced" by the module before it reaches the memory; and

data transfer control means for controlling data transfer from said bridge module to said management modules so that, after said data is transferred to the two management modules corresponding to said two transferred-to addresses, said data is written at said written-in address in said cache memory of each of the two management modules (Fig. 2, the host (108) can write and read data to and from the storage system via the host interface (the combination of 204 and 206) to the bridge (208), through the device interface (138.1) – col. 7, line 47 through col. 8, lines 39). Again, it is worthy to note that even though Weber teaches storing in the disks rather than the cache, an obvious variation of Weber's apparatus would include Hauck's storage system, as per the discussion *supra* (per claims 13 and 27). When the host writes to the storage system, the data is mirrored in Hauck's system such that at least two addresses (one for each controller's cache) are written-in to.

Weber additionally teaches one of the two management modules as including management means for managing information on the management module which is in

mirror relation to the other management module and for managing the association between a master area address in said cache memory of the one second management module and a mirror area address in said cache memory of the other second management module being in the mirror relation to this management module - referring to Fig. 2, host write 1 data (230) is written to controller 2 (i.e. mirrored), and likewise host write data 2 (270) is mirrored to controller 1 – paragraph 0039-0040 all lines. Additionally, Weber teaches (referring to Fig. 4) a master area for each cache is maintained (Read/Write/Copy Cache). The controllers maintain cache coherency by transmitting and receiving metadata, which comprise a bit map and cache identifier. These data allows the controllers to maintain their respective hash tables (Fig. 4, elements 490 and 495) which allows the controllers to maintain where cache lines are present in the cache area, and also maintain a free list of mirror locations (paragraphs 0045-0048, all lines).

Though Weber teaches multiple management modules (disks (106) within the disk storage system (104)), he fails to teach said modules containing cache used to mirror data.

Hauck however teaches an apparatus for maintaining cache coherency in a storage system, which includes a storage system (Fig. 1, elements 110, 112 ... 118, 120, 130 and 160) including a plurality of control units (Fig. 1, element 110, 112, ... 118). Referring to Fig. 2, each control unit (i.e. controller) contains a cache area (270), and a cache copy area (280) – paragraph 0039, all lines. Since Hauck's controllers

inherently controller access to the storage system, they assert at least some control over the control system.

Neither Hauck nor Weber teach a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second module is full, at which time a mirror area of said one second module are written.

Avraham however teaches an appliance including a FLASH memory in which a second memory module is written with all or part of a first memory module's data once it is determined that the first memory module is full (paragraph 0054, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory in to his own scalable memory. By doing so, Weber would have a more robust memory

system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

8. Claims 2-4, 9-12, 16-18 and 23-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the combined teachings of Weber (US Patent 5,937,174), Hauck (US PG Publication 2003/0158999 A1), and Avraham (US PG Publication 2004/0103238 A1) as applied to claims 1 and 15 above respectively, and in further view of Hashimoto et al. (US PG Publication 2002/0016898 A1), hereinafter Hashimoto.

As for claims 2-3 and 16-17, though the combined teaches of Weber, Hauck and Avraham teach all the limitations of claim 1 and 15 above, they fails to teach the limitations of claims 2 and 3. Hashimoto further teaches designating, in said addressing information, a page address in said cache memory of each of said management modules and an offset address in a page designated by said page address, as said written-in address for said data in said cache memory, and specific information for specifying said two management modules having said cache memories in which said data is to be actually written, as said two transferred-to addresses for said data (Hashimoto discusses address conversion circuitry for both the first and second addresses. The address conversion circuitry uses the generated address and an offset (inherent for the conversion to take place) to generate appropriate addresses, in order to access the memories, paragraph 0019-0020, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further incorporate Hashimoto's host interface device into his own memory structure for high data bandwidth RAID applications. By doing so, Weber

would have a more efficient means of interfacing from his host to bridge unit, which includes reducing the power consumption caused by excessive signal transition on the address bus as taught by Hashimoto in paragraphs 0013 and 0017, all lines.

As for claims 4 and 18, Weber teaches interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two management modules are designated as said specific information (col. 8, lines 20-39).

It is worthy to note that since Weber only teaches one bus line, the addresses generated by Hashimoto could only refer to the one address bus that is used to transfer the data specified by the generated addresses.

As for claims 9-12 and 23-26, Hauck teaches a case in which a capacity of a master area of said cache memory is full when data read out from said disk unit through said disk interface module and said bridge module is temporarily preserved in the cache memory, each of said management modules preserves the readout data in a mirror area of said cache memory of the management module, which is in the mirror relation to this management module, on the basis of a situation of management by said management means (Hauck discusses the system's ability to preserve data by reading out the data from a survivor controller (referring to Fig. 7, element 710) and reading into a replacement controller (730) to preserve data that was stored in the failed controller (720). This process takes place in case of a controller failure, or if a large ownership of data is shouldered by the controller (i.e. cache becomes full) – paragraph 0054-0056, all lines).

It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Hauck's apparatus for maintaining cache coherency in his own system for RAID storage. By doing so, Weber would have a solution to the need for data stored in a storage device to be accessed redundantly through an alternative device controller in the event that a controller fails (paragraph 0008, all lines as taught by Hauck). Furthermore, Hauck's system would have a far more efficient system by providing a means for minimizing the number of messages required to manage a coherent cache, and eliminate the need to flush data to backing disks as taught in paragraph 0019, all lines.

Response to Arguments

9. Applicant's arguments have been fully considered however they are not persuasive.

Under the heading, "REJECTIONS OF CLAIM 32 UNDER 35 U.S.C. § 102", Applicant asserts, "[c]laim 32 has been amended to recite that the storing data initially directed to the master area is 'from said data input request' to clarify this feature. In contrast, the data written in Avraham is not from a data input request, but rather the entire contents of a full cache memory module. Thus Applicants respectfully submit that Avraham does not teach or suggest the recited features of claim 32."

This argument however is not persuasive. The claim sets forth a process comprising two steps. A determining step to determine if a master area of a first

memory module is “sufficient” for an input request; and a storing step, which stores data directed to the master from the input request, to a mirrored area of a second memory module. Examiner maintains that Avraham in fact anticipates this claim in light of the newly added claim limitations. For example (referring again to paragraph 0054, all lines), the determining step is met once the system checks to see if the cache is full. That is, every time a new write request is received, the cache is checked to see if it is full (see Fig. 3). The storing step is met by Avraham's process step of transferring data from the volatile memory to the nonvolatile memory. That is, data that is stored in the volatile memory was originally “from the data input request” for it to be stored in the volatile memory, therefore the data stored in the nonvolatile memory (after the transfer from volatile to nonvolatile memory is complete) comprises data once directed to the master area of the first memory, from the data input request from which a determination was made to see if the master area of the volatile memory was “sufficient”. As such, Avraham anticipates claims 32 as per the arguments and rejections discussed *supra*.

Under the heading, “REJECTIONS OF CLAIMS 1-4,9-13,15-18,23-27 AND 29-30 UNDER 35 U.S.C. § 103”, Applicant contends (as for claims 13, 27 and 30), “nowhere in Weber is taught or described ‘a bridge module connected through an interface bus to said first and second modules’ - the second modules each having a cache memory. First, Weber describes communication with a *disk storage system* and not cache. Second, the bus bridge 206 is connected to the high speed host interface 204, and transfers data to a main memory controller 212, not to the device/disk

interfaces 138.1. The bus bridge 206 of Weber communicates with the high speed host and main memory controller only. See col. 8, lines 27-32. Weber describes that it is the bus bridges 208 and 210 (bridges not connected to the high speed host interface 204) that provide the exchange of information between RAID array 104 and high speed cache buffer under the control of main memory controller 212."

This argument however is not persuasive. First, Examiner notes that Weber's bus bridge 208 is connected to the device I/F (138.1) via bus (250) and to the high speed host I/F via bus (252). Referring to the lines cited by Applicant, bus bridge (208) sends data from bus (252) to the disks (104) via the device I/F (138.1). The data on that bus is communicated in part from the host. Examiner further notes that the previous argument is not persuasive as Examiner cited the *combination* Weber, Hauck and Avraham's disclosures to meet these limitations, not Weber alone. Applicant is reminded, "[o]ne cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981), pursuant to MPEP § 2145 (IV.).

Continuing under this heading, Applicant asserts, "Weber describes a bus bridge that connects to other modules only through other bridge modules, Weber does not teach or suggest the features of claims 13, 27 and 30 [that is, the feature including connecting a bridge module to first and second modules *without* connecting through any other bridge modules]."

This argument however is not persuasive. Examiner currently maps the combined elements high speed I/F (204) and the bus bridge (206) to read on Applicant's interface module. Based on this interpretation, the bus bridge (208) is now connected to the device I/F and the high speed host I/F through busses (250) and (252) respectively, without the need to pass through another bus bridge. In other words, data from the host (108) travels to the host bus (120) to the host I/F (204 + 206) to the bridge bus (252) to the bridge (208) to the interface bus (250) and finally to the interface module (138.1). Since the host interface "ends" at busses 250 and 252, said interface is connected to the device interface through at most, one bridge unit (namely element 208).

Applicant further cites salient portions of claims 27 and 30, and sets forth a generic argument that they are allowable. This argument lacks specifics as to how or why Applicant believes these claims overcome the cited art, therefore they are not persuasive.

Continuing on page 15 of Applicant's remarks (as for claim 1), Applicant again asserts that Weber's "bus bridge" that is connected to the high speed host interface is not connected to the device/disk interfaces. This argument however is not persuasive, as Examiner clearly demonstrates those connections in Fig. 2 of Weber as per the rejections and arguments presented *supra*.

Applicant further contends, "each of the bus bridges in Weber 'adapts the signals applied to their respective, unique, connected bus architecture to the intermediate

shared memory bus.' See col. 8, lines 23-26. Thus, the purpose of these buses is to convert a signal from one bus to another, and nothing about addresses for designation of two second modules is taught or suggested here."

This argument however is not persuasive. First, Examiner is unclear what specific limitation/s of the instant claims recite the feature Applicant alleged is deficient in Weber's teachings. Though Applicant failed to provide the specific recitation for which is being argued for, Examiner assumes Applicant is referring to the recitation of "said first module including address designation means for producing addressing information to designate two written-in destinations for writing data to be written" in lines 7-8 of claim 1 for example. Examiner however maintains that Weber in view of Hauck and in further view of Avraham teach this limitation. More specifically, the disks depicted in Fig. 2 of Weber's disclosure are manipulated via the bus bridge through the disk interface. In order to access the disks, data, control, and address information must be present on the bus; else the system would not be able to correctly access the disks. In other words, Weber's system would fail to execute its intended function should address information not be "produced" and transmitted to the memories.

Applicant reasserts on this page (page 15) of the remarks that none of Weber, Hauck, Avraham and Hashimoto teach "a bridge module connected ... without connecting through any other bridge modules." Examiner fails to find this argument persuasive as per the rejections and arguments discussed *supra*.

Applicant further cites salient portions of claims 15 and 29, and sets forth a generic argument that they are allowable. This argument lacks specifics as to how or why Applicant believes these claims overcome the cited art, therefore they are not persuasive.

Applicant finally asserts that all dependant claims are allowable for at least further limiting the base claims which are alleged to overcome the cited art. This argument however is not persuasive, as Examiner maintains that each base claim is rendered obvious by the cited art as per the rejections and arguments discussed supra.

As for claim 33, Applicant failed to provide any specific arguments with regard to distinguishing features of the instant with respect to the previously cited prior art (just set forth a generic argument of allowability). Since Examiner has no formal argument to respond to, Examiner maintains that claim 33 is rejected for the reasons discussed in the rejections set forth above.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Craig E. Walter whose telephone number is (571) 272-8154. The examiner can normally be reached on 8:30a - 5:00p M-F.

12. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on (571) 272-6799. . The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

13. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Craig E Walter
Examiner
Art Unit 2188

CEW

HYUNG S. SOUGH
SUPERVISORY PATENT EXAMINER
12/09/07